

Serial No. 09/277,893

**REMARKS**

The Final Office Action mailed on November 27, 2001, has been received and reviewed. Claims 17-33, 50-72, and 74-101 are currently pending in the application. Each of claims 17-33, 50-72, and 74-101 stands rejected.

It is proposed that claims 17, 50, and 71 be amended as presented herein.

Reconsideration of the above-referenced application is respectfully requested.

**Information Disclosure Statement**

Please note that a Supplemental Information Disclosure Statement was filed in the above-referenced application on November 21, 2001, and that no copy of the accompanying PTO-1449 has yet been returned to the undersigned attorney. It is respectfully requested that the references cited in the Supplemental Information Disclosure Statement be considered and made of record in the above-referenced application and that an initialed copy of the PTO-1449 evidencing the same be returned to the undersigned attorney.

**Rejections Under 35 U.S.C. § 103(a)****Fischer in View of Sandhu**

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Serial No. 09/277,893

Claims 17 and 19-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,185,291 to Fischer et al. (hereinafter "Fischer") in view of U.S. Patent 5,231,056 to Sandhu (hereinafter "Sandhu").

Fischer teaches a fuse for use in a semiconductor device structure, as well as a process for fabricating the fuse. The fuse of Fischer, which is disposed over an insulative structure (dielectric 10, *see, e.g.*, FIGs. 1-4; col. 2, lines 29-36), includes a first conductive layer 11 and a second conductive layer 12. The first conductive layer 11 of the finished fuse may be formed from aluminum or tungsten (col. 2, lines 43-45) and includes two spaced apart end regions (FIG. 3). The second conductive layer 12 of the fuse is preferably formed from the same material as the first layer 11, but may also be formed from polysilicon (col. 2, lines 59-63). In a finished fuse, such as that illustrated in FIG. 3 of Fischer, end portions of the second conductive layer 12 overlie the spaced apart regions of the first conductive layer 11, while the central portion 111 of the second conductive layer 12 is located in substantially the same plane as the first conductive layer 11 and between the spaced apart portions of the first conductive layer 11 (*see also*, col. 2, lines 56-58).

Fischer teaches that the fuse may be fabricated by forming a first layer of conductive material 11 over an insulative structure 10 (FIG. 1; col. 2, lines 45-48), patterning a "window" 111 in the first layer of conductive material to expose a portion of the underlying insulative structure (FIG. 1; col. 2, lines 36-38; col. 3, lines 34-55), forming a second layer 12 of conductive material over the first layer 11 and within the window 111 (FIG. 2; col. 2, lines 49-55), and patterning the "combined" first and second layers to form the fuse (FIG. 3; col. 2, lines 56-58).

The fuse of Fischer is designed to rupture upon exposure of the central region of the second conductive layer to a laser beam (col. 4, lines 58-65).

Sandhu teaches a chemical vapor deposition (CVD) method for forming tungsten silicide. Sandhu suggests that the method may be useful in transistor gate fabrication processes for forming a polycide (i.e., polysilicon-tungsten silicide) gate structure.

Serial No. 09/277,893

Independent claim 17, as proposed to be amended herein, recites a method for fabricating a fuse. The method of claim 17 includes, among other things, patterning a layer of conductive material to define at least two laterally distinct, spaced apart regions, between and around which an underlying insulative structure is exposed. The method of claim 17 also includes disposing a layer of metal silicide over and between the two regions of conductive material.

*One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination*

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer and Sandhu in the manner that has been asserted in the outstanding Office Action.

Specifically, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to substitute the metal silicide formation process described in Sandhu for the formation of an aluminum, tungsten, or polysilicon layer in the fuse fabrication process described in Fischer, thereby using metal silicide in place of the aluminum, tungsten, or polysilicon of Fischer as the portion of a fuse that is to be ruptured.

While it is acknowledged that metal silicides are known to provide "low bulk resistance and low stress", this fact in and of itself would not have motivated one of ordinary skill in the art to substitute the use of tungsten silicide for materials such as aluminum or tungsten, particularly since the aluminum, tungsten, or polysilicon of Fischer is used in the portion of a fuse that is to be ruptured upon "programming" the fuse, where some bulk resistance and/or stress may be desirable to facilitate blowing of the fuse and, thus, programming thereof at a particular programming voltage. By touting the usefulness of aluminum, tungsten, and polysilicon as the second, programmable material layer of the fuse disclosed therein, Fischer clearly fails to provide any motivation to one of ordinary skill in the art to find a substitute for these materials.

Also, based on the admission in the outstanding Office Action that the only teaching that has "been gleaned from Sandhu is the teaching of tungsten silicide as a well known conductive

Serial No. 09/277,893

material", it is clear that the Examiner does not himself believe that Sandhu would have motivated one of skill in the art to substitute tungsten silicide or any other metal silicide for the aluminum, tungsten, or polysilicon of the second conductive layer of the Fischer fuse. Nor has any other art been cited to indicate why one of ordinary skill in the art would have been motivated to change the conductive material of the second conductive layer of the Fischer fuse.

It is, therefore, respectfully submitted that one of ordinary skill in the art would not have been motivated to modify the fuse fabrication method described in Fischer by forming a metal silicide layer, such as by the process taught in Sandhu, rather than the polysilicon layer described in Fischer. Consequently, it appears that any motivation to combine the teachings of Fischer and Sandhu could only have been based on hindsight provided by the specification or claims of the referenced application.

*The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element*

It is further submitted that the combination of Fischer and Sandhu fails to teach or suggest each and every element of independent claim 17.

In contrast to the subject matter recited in independent claim 17, neither Fischer nor Sandhu, taken alone or in combination, teaches a fuse fabrication method that includes patterning a layer of conductive material to form at least two laterally discrete, spaced apart regions with an underlying insulative structure exposed therethrough and formed therearound. Rather, the teachings of Fischer are limited to forming a *window* centrally through a conductive layer, which could not result in laterally discrete, spaced apart regions of a first layer of conductive material around and between which an underlying insulative structure is exposed. According to Fischer, no laterally discrete, spaced apart regions of the first layer of conductive material are formed until after the second layer of conductive material has been formed and, thus, the underlying insulative structure is never exposed between these laterally discrete, spaced apart regions of the first layer of conductive material.

Sandhu neither teaches nor suggests a fuse fabrication method.

Serial No. 09/277,893

As neither Fischer nor Sandhu teaches or suggests patterning a layer of conductive material to define two or more laterally discrete, spaced apart regions of conductive material with an insulative structure exposed therebetween, it would be impossible to combine these references to teach patterning a layer of conductive material in such a fashion.

*No Reasonable Expectation of Success*

Moreover, even assuming, *arguendo*, that one of ordinary skill in the art would have been motivated to combine the teachings of Fischer and Sandhu in the manner that has been asserted in the outstanding Office Action, it is respectfully submitted that one of ordinary skill in the art would not reasonably expect that Fischer and Sandhu could be successfully combined in such a way as to render obvious the subject matter recited in amended independent claim 17. Again assuming, for the purpose of argument, that the asserted combination of Fischer and Sandhu might result in the same structure as a structure that may be formed by the method recited in amended independent claim 17, the combination of Fischer and Sandhu could not result in a method in which a layer of conductive material is patterned "to define at least two laterally discrete, spaced apart regions of conductive material between and around which [an underlying] insulative structure is exposed . . ."

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 17 is allowable over the combination of Fischer and Sandhu.

Claims 19-33 are each allowable, among other reasons, as depending either directly or indirectly from claim 17, which is allowable.

In view of the foregoing, it is respectfully requested that the Office withdraw the rejections of claims 17 and 19-33 under 35 U.S.C. § 103(a).

Serial No. 09/277,893

Fischer in View of Sandhu and Further in View of Szluk

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Sandhu, as applied to claim 17 above, and further in view of U.S. Patent 4,647,340 to Szluk et al. (hereinafter "Szluk").

The teachings of Fischer and Sandhu have been summarized above.

Szluk teaches a so-called "antifuse", which differs in structure and function from a fuse, and a method for fabricating the antifuse. As shown in FIG. 5 of Szluk, the antifuse of Szluk includes a conductively doped region 17 of a semiconductor substrate and a conductive element, which includes a polysilicon layer 22 (FIG. 3) and an overlying tungsten layer 34 that extends close to the conductively doped region, but is separated therefrom by way of a thin dielectric structure 39. A contact structure 37 communicates with the conductively doped region 17 of the substrate.

Upon applying a sufficient voltage to the contact structure, the thin dielectric structure 39 that electrically isolates the conductively doped region 17 of the substrate from the tungsten layer 34 of the conductive element ruptures, facilitating electrical communication between the conductively doped region 17 of the substrate and the conductive element 22/34 and enabling the antifuse to conduct an electrical current thereacross (col. 2, lines 27-33).

The antifuse of Szluk may be fabricated concurrently with the fabrication of a transistor gate structure (col. 2, lines 34-63). Once the substrate is conductively doped at regions 17, a dielectric layer 26 is patterned to form a so-called "programming oxide", which is the illustrated thin dielectric layer 39 (FIG. 3; col. 4, lines 46-52). A tungsten layer 36 that overlies the polysilicon layer 22 is then formed and patterned.

Claim 18 is allowable, among other reasons, as depending from claim 17, which should be allowed.

It is also respectfully submitted that there are several additional reasons that the combination of Fischer, Sandhu, and Szluk does not render the subject matter recited in claim 18 obvious.

Serial No. 09/277,893

*One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination*

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Szluk with those of either Fischer or Sandhu. In particular, when the teachings of Szluk are considered in their entirety, as required by M.P.E.P. § 2141.02, it is not understood how or why one of ordinary skill in the art would have been motivated to incorporate teachings from a reference (Szluk) which teaches a method for fabricating an antifuse, which, prior to be "programmed", includes the fabrication of an insulative structure to block the flow of electrical current thereacross, into a reference (Fischer) that teaches a method for fabricating a fuse that, prior to being "programmed", is configured to convey an electrical current thereacross.

In any event, Szluk does not supply the motivation that is missing from both Fischer and Sandhu to fabricate a second conductive layer of a fuse from a metal silicide rather than from aluminum, tungsten, or polysilicon.

*There Is No Reasonable Expectation that the Proposed Combination Would Be Successful*

It is also respectfully submitted that there is no reasonable expectation that the combination of Fischer, Sandhu and Szluk would be successful.

In addition to the fact that, by combining Fischer and Sandhu, a fuse fabrication method that lacks patterning of a "layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which [an underlying] insulative structure is exposed", it is respectfully submitted that one of ordinary skill in the art could not reasonably expect the combination of Fischer with Szluk to successfully result in the method recited in claim 18. Of particular note are the vast differences between the types of devices disclosed in Fischer and Szluk. While Fischer discloses a fuse, with a member that ruptures, is blown, or otherwise becomes discontinuous when "programmed" with a laser and, thus, has a

Serial No. 09/277,893

diminished ability to conduct an electrical signal, Szluk teaches an antifuse which does not conduct an electrical signal until programmed with a sufficient voltage.

Because of these vast differences, as well as the direction provided in M.P.E.P. § 2141.02 that the teachings of each reference must be considered in their entirety, it is respectfully submitted that there is no reasonable expectation that the combination of a method for forming an antifuse (Szluk) could be incorporated into a method for forming a fuse (Fischer) to render obvious a method for fabricating a fuse which includes the elements of claim 18. Rather, such a fuse would include an insulative element that prevents the flow of electrical current thereacross.

Moreover, as the antifuse fabrication method described in Szluk lacks patterning of a "layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which said insulative structure is exposed", it is respectfully submitted that any combination of Fischer, Sandhu, and Szluk would fail to result in the method recited in claim 18 and amended independent claim 17 from which claim 18 depends.

Accordingly, it is respectfully submitted that there is no reason to expect that the proposed combination of Fischer, Sandhu, and Szluk would successfully result in a method for fabricating a fuse.

*The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element*

Moreover, with respect to the antifuse fabrication process described in Szluk, there is no teaching or suggestion of patterning a conductive layer, such as the polysilicon layer thereof, to form at least two laterally discrete, spaced apart regions between and around which regions of an underlying insulative structure are exposed. As each of Fischer, Sandhu, and Szluk fails to teach or suggest this element of claims 17 and 18, it is respectfully submitted that the Fischer, Sandhu, and Szluk cannot in combination teach or suggest this element.



Serial No. 09/277,893

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 18 is allowable over the combination of Fischer, Sandhu, and Szluk and requested that the rejection of claim 18 under 35 U.S.C. § 103(a) be withdrawn.

Fischer in View of Szluk and Sandhu

Claims 50, 51, and 55-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Szluk and Sandhu.

The teachings of each of these references have been summarized previously herein.

*One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination*

For the same reasons provided above with respect to claim 18, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer, Sandhu, and Szluk in the manner that has been suggested in the outstanding Office Action.

*There Is No Reasonable Expectation that the Proposed Combination Would Be Successful*

In addition, for the same reasons provided above with respect to claim 18, it is respectfully submitted that there is no reasonable expectation that the combination of Fischer, Szluk, and Sandhu would be successful in rendering obvious the method for fabricating a fuse as recited in claims 50, 51, and 55-68.

*The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element*

Moreover, it is respectfully submitted that Fischer, Szluk, and Sandhu, taken either alone or in combination, do not teach or suggest each and every element of claims 50, 51, and 55-68.

Independent claim 50, as proposed to be amended herein, recites a method for fabricating a fuse that includes, among other things, fabricating laterally discrete, spaced apart regions

Serial No. 09/277,893

comprising polysilicon on an insulative structure and fabricating a fuse comprising a metal silicide. When the laterally discrete, spaced apart regions are fabricated, and before the overlying fuse is formed, an insulative layer that underlies the spaced apart regions comprising polysilicon is exposed between and around the spaced apart regions. The fuse is fabricated in such a way as to include a central region located adjacent the insulative structure and between the spaced apart regions, as well as at least two terminal regions on opposite ends of the central region and adjacent the spaced apart regions that comprise polysilicon.

The teachings of Fischer are limited to forming a *window* centrally through a conductive layer, which could not result in *laterally discrete, spaced apart* regions of a first layer of conductive material. When the second conductive layer is formed, the insulative structure is no longer exposed through the window. According to Fischer, the first layer of conductive material is not patterned to form laterally discrete, spaced apart regions until after the second layer of conductive material has been formed and covers any portions of the insulative structure that were previously exposed through the window. Further, in the method of Fischer, the insulative structure that underlies the conductive structure is not exposed *around* the subsequently formed laterally discrete, spaced apart regions until after the second conductive layer has been formed thereover and patterned.

In addition, Fischer teaches that polysilicon may be used to form a top layer of the fuse described therein, including the fusible element that extends between terminals of the fuse. Fischer does not teach or suggest that spaced apart regions may be formed from polysilicon.

Sandhu neither teaches nor suggests a fuse fabrication method.

The antifuse fabrication method disclosed in Szluk does not include forming laterally discrete spaced apart regions of any conductive material, let alone polysilicon.

As none of Fischer, Sandhu, or Szluk teaches or suggests a fuse fabrication method which includes "fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions", as is recited in independent claim 50, as proposed

Serial No. 09/277,893

to be amended, it is respectfully submitted that there is no way for the combination of these references to teach or suggest this element of amended independent claim 50.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 50 is allowable over the combination Fischer, Sandhu, and Szluk.

Each of claims 51 and 55-68 is allowable, among other reasons, as depending either directly or indirectly from claim 50, which is allowable.

Therefore, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 50, 51, and 55-68 be withdrawn.

Fischer, Szluk, Sandhu, and Degelormo

Claims 52-54, 69, and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer, Szluk, and Sandhu, as applied to claims 50 and 51 above, and further in view of U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo").

The teachings of Fischer, Szluk, and Sandhu have been summarized previously herein.

Degelormo merely teaches a chemical vapor deposition method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, let alone laterally discrete, spaced apart regions comprising polysilicon over an insulative structure around and between which an underlying insulative structure is exposed.

Thus, Degelormo includes no teaching or suggestion that would remedy the deficiencies of Fischer, Szluk, and Sandhu with respect to their inability to have provided one of ordinary skill in the art with motivation to make the asserted combination.

Nor do the teachings of Degelormo provide one of ordinary skill in the art with any additional reason to believe that the teachings of Fischer, Szluk, Sandhu, and Degelormo could be successfully combined to provide a method for fabricating a fuse. In particular, Degelormo does not include any teaching or suggestion of "fabricating laterally discrete, spaced apart regions

Serial No. 09/277,893

comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions", an element of the fuse fabrication process recited in amended claim 50, from which claims 52-54, 69, and 70 depend, which is also missing from Fischer, Sandhu, and Szluk.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claims 52-54, 69, and 70, each of which depends from claim 50, are allowable over the combination of Fischer, Szluk, Sandhu, and Degelormo.

Further, each of claims 52-54, 69, and 70 is allowable, among other reasons, as depending either directly or indirectly from claim 50, which is allowable.

Therefore, it is respectfully requested that the Office withdraw the rejection of claims 52-54, 69, and 70 under 35 U.S.C. § 103(a).

#### Szluk in View of Bohr and Fischer

Claims 71, 74-86, 88-92, and 101 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk in view of Bohr and Fischer.

The teachings of Szluk and Fischer have been summarized previously herein.

As shown in FIG. 1A of Bohr, Bohr teaches a fuse 100 that includes a polysilicon layer 105 and an overlying metal silicide layer 104, as well as a method for fabricating the fuse. As depicted in FIG. 1A of Bohr, both the polysilicon layer 105 and the metal silicide layer 104 extend the complete length of the fuse 100. The fuse is "blown" when a sufficient voltage is applied to the metal silicide layer to cause the metal silicide to agglomerate, rendering the metal silicide layer discontinuous at some point along the length of the fuse (FIG. 2A; col. 4, lines 17-36). As a result of being blown, an electrical current must traverse the fuse through the remaining polysilicon layer, which has a greater resistance than the metal silicide layer (col. 4, lines 37-39).

It is respectfully submitted that there are several reasons a *prima facie* case of the obviousness of claims 71, 74-86, 88-92, and 101 has not been established.

Serial No. 09/277,893

*One of Ordinary Skill in the Art Would Not Have Been Motivated to Make  
the Proposed Combination*

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Szluk, Bohr, and Fischer in the manner that has been suggested in the outstanding Office Action.

Szluk, Bohr, and Fischer teach methods for fabricating three very different types of fuses. Szluk teaches an antifuse that includes a dielectric structure that is blown when a sufficient voltage is applied to the antifuse, causing the antifuse to more readily convey an electrical current. Thus, the fabrication method of Szluk includes forming the dielectric structure.

Bohr teaches a fuse that conveys an electrical current until it is blown by applying a sufficient voltage thereacross, increasing the fuse's resistance to the flow of an electrical current thereacross. The method disclosed in Bohr includes forming a fusible element that includes an upper metal silicide layer and a lower polysilicon layer.

Fischer teaches a fuse that is programmed with a laser rather than with an electrical current. Fabrication of this fuse includes the formation of a fusible element from aluminum, tungsten, or polysilicon.

The structures of Szluk, Bohr, and Fischer operate in different manners because of diversities between the features thereof. Very different fabrication processes are required to form the diverse features of the structures of Szluk, Bohr, and Fischer. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to apply the fabrication processes of any of these fuses to the fabrication processes of any of the others of these fuses in a way that would have rendered obvious the presently claimed method.

It is further submitted that any motivation to combine the teachings of Fischer, Szluk, and Bohr in the manner that has been set forth in the outstanding Office Action could only have been gleaned from the hindsight provided by the specification and claims of the referenced application.

Serial No. 09/277,893

*Bohr Teaches Away from The Subject Matter of the Claims*

Second, it is respectfully submitted that Bohr teaches away from the method recited in amended independent claim 71.

In pertinent part, M.P.E.P. § 2141.02 provides:

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc., v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). (Italicized emphasis supplied).

Independent claim 71, as proposed to be amended herein, recites a method that includes patterning regions of a layer of polysilicon to form laterally discrete, spaced apart regions of polysilicon around and between which an underlying field oxide region is exposed. Rather than teach a method for forming a fuse in which such laterally discrete, spaced apart regions of polysilicon are formed, when Bohr is considered in its entirety, it teaches a method for fabricating a fuse that includes a polysilicon, or lower conductive, layer that extends across the entire fuse, including the narrowed region thereof. Therefore, it is respectfully submitted that Bohr teaches away from the method recited in amended independent claim 71.

*There Is No Reasonable Expectation that the Proposed Combination Would Be Successful*

Third, it is respectfully submitted that there is no reasonable expectation that the combination of Szluk with Bohr and Fischer would successfully result in a method for fabricating a fuse, as is recited in claims 71, 74-86, 88-92, and 101.

Bohr teaches a fuse fabrication method that lacks any teaching or suggestion of "patterning at least regions of [a] layer of polysilicon disposed over at least one field oxide region . . . to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween . . .", which element is also missing from Fischer and Szluk.

Serial No. 09/277,893

Accordingly, it is respectfully submitted that any combination of the teachings of Szluk, Bohr, and Fischer could not reasonably be expected by one of ordinary skill in the art to result in the method recited in independent claim 71 or any of claims 74-86, 88-92, or 101 which depend therefrom.

Therefore, it does not appear that one of ordinary skill in the art could reasonably expect that a combination of the methods of Szluk, Bohr, and Fischer in the manner that has been asserted in the outstanding Office Action would be successful.

*The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element*

Fourth, it is respectfully submitted that Szluk, Bohr, and Fischer, taken either alone or in combination, do not teach or suggest each and every element of amended independent claim 71.

Specifically, none of Szluk, Bohr, or Fischer teaches or suggests a fuse fabrication method that includes "patterning at least regions of [a] layer of polysilicon disposed over at least one field oxide region . . . to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween" or "disposing a layer of metal silicide on said layer of polysilicon and into contact with said [exposed] portions of said at least one field oxide region".

Rather, the teachings of Fischer are limited to forming a window centrally through a conductive layer, which could not result in *laterally discrete, spaced apart* regions of a first layer of conductive material around and between which an underlying insulative structure is exposed. According to Fischer, no laterally discrete, spaced apart regions of the first layer of conductive material are formed until after the second layer of conductive material has been formed.

Sandhu neither teaches nor suggests a fuse fabrication method.

In the fabrication method of Bohr, polysilicon is not patterned in such a way as to define at least two spaced apart regions but, rather, to form a layer that extends completely across the resulting fuse, including the narrowed fusible element thereof.

Serial No. 09/277,893

As none of Szluk, Bohr, or Fischer teaches or suggests patterning at least regions of a layer of polysilicon in the manner recited in independent claim 71, as proposed to be amended, any combination of these references also fails to teach or suggest this element of amended claim 71.

In view of the foregoing, it is respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 71 is allowable over the combination of Fischer, Szluk, and Bohr.

Claims 74-86, 88-92, and 101 are each allowable, among other reasons, as depending either directly or indirectly from claim 71, which should be allowed.

For the foregoing reasons, it is respectfully requested that the Office withdraw the 35 U.S.C. § 103(a) rejections of claims 71, 74-86, 88-92, and 101.

Szluk, Bohr, Fischer, and Degelormo

Claim 72 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk, Bohr, and Fischer, as applied to claim 71 above, and further in view of Degelormo.

Claim 72 is allowable, among other reasons, as depending from claim 71, which should be allowed.

Szluk, Bohr, Fischer, and Sandhu

Claim 87 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk, Bohr, and Fischer, as applied to claim 71 above, and further in view of Sandhu.

The teachings of Szluk, Bohr, Fischer, and Sandhu have been summarized previously herein. Again, Sandhu merely teaches a process by which tungsten silicide may be formed.

Claim 87 is allowable as depending from claim 71, which should be allowed, for the same reasons provided above with respect to claim 71 and, further, because Sandhu does not provide the motivation that would be necessary to combine the teachings of Szluk, Bohr, and Fischer.



Serial No. 09/277,893

Szluk, Bohr, Fischer, and Ukeda

Claims 93-100 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Szluk, Bohr, and Fischer, as applied to claim 71 above, and further in view of U.S. Patent 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

The teachings of each of Szluk, Bohr, and Fischer have been summarized previously herein.

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used in fabricating a fuse.

Accordingly, it is clear that Ukeda does not remedy the deficiencies of Szluk, Bohr, Fischer, and the knowledge that was generally available in the art prior to the filing date of the above-referenced application with respect to providing some motivation to one of ordinary skill in the art to combine the teachings of these references. It is also clear that Ukeda does not include any teaching that would give one of ordinary skill in the art a reasonable basis for expecting the combination of Szluk, Bohr, Fischer, and Ukeda to provide a successful method for fabricating a fuse.

Claims 93-100 are each allowable, among other reasons, as depending directly or indirectly from claim 71, which should be allowed. Claims 93-100 are also allowable since Ukeda does not supply the motivation that would be required to combine the teachings of Szluk, Bohr, and Fischer.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 93-100 be withdrawn.

Serial No. 09/277,893

**ENTRY OF AMENDMENTS**

It is respectfully requested that the claim amendments that have been proposed herein be entered because none of the proposed amendments adds new matter to the claims. Moreover, it is respectfully submitted that, since the proposed claim amendments merely clarify the previously claimed subject matter, none of the proposed amendments would require an addition search. Finally, if it is determined that the proposed amendments do not place the application in condition for allowance, entry thereof is respectfully requested upon filing of a Notice of Appeal herein.

**CONCLUSION**

It is respectfully submitted that each of claims 17-33, 50-72, and 74-101 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing the allowance of any of claims 17-33, 50-72, and 74-101 remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully Submitted,



Brick G. Power  
Registration Number 38,581  
Attorney for Applicant  
TRASKBRITT, PC  
P.O. Box 2550  
Salt Lake City, Utah 84110  
Telephone: (801) 532-1922

Date: January 11, 2002

Enclosure: Version With Markings to Show Changes Made

BGP/hlg:djp

N:\2269\3543\Amendment Final 2.wpd

Serial No. 09/277,893

**VERSION WITH MARKINGS TO SHOW CHANGES MADE****IN THE CLAIMS:**

Please amend the claims as follows:

17. (Amended four times) A method of fabricating a fuse upon a semiconductor device, comprising:

disposing a layer of conductive material over an insulative structure of the semiconductor device; patterning said layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which said insulative structure is exposed;

disposing a layer of metal silicide over the semiconductor device, including adjacent to said at least two regions and to said insulative structure exposed between and around said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

50. (Amended four times) A method of fabricating a fuse, comprising: fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions; and

fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent said spaced apart regions.

Serial No. 09/277,893

71. (Amended four times) A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor substrate, including over said layer of insulative material and over field oxide regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed over at least one field oxide region of said field oxide regions to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with [a portion] portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween;

disposing a layer of metal silicide on said layer of polysilicon and into contact with said [portion] portions of said at least one field oxide region;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.